Title: Modelling and Simulation of IEEE 24 Bus system using Modelica and OpenIPSL

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Abstract: The IEEE 24-bus test system shall be used to study the voltage stability at different buses. The power system model consists of 10 generators, one synchronous condenser 24 buses, 16 loads, 34 lines, 5 transformers. The system is on a 100 MVA base. The model submitted is implemented in Modelica language using OpenIPSL package shown in Figure 1. A fault simulated at Bus 11 for the duration of 0.4 seconds (4 seconds to 4.4 seconds), the simulated voltage profiles of IEEE 24 bus system at various buses shown in Figure 2. For all analysis of this system, the lower voltage magnitude limits at all buses are 0.95 p.u and upper limits are 1.05 p.u. Simulation obtained shows voltage profiles at various buses.

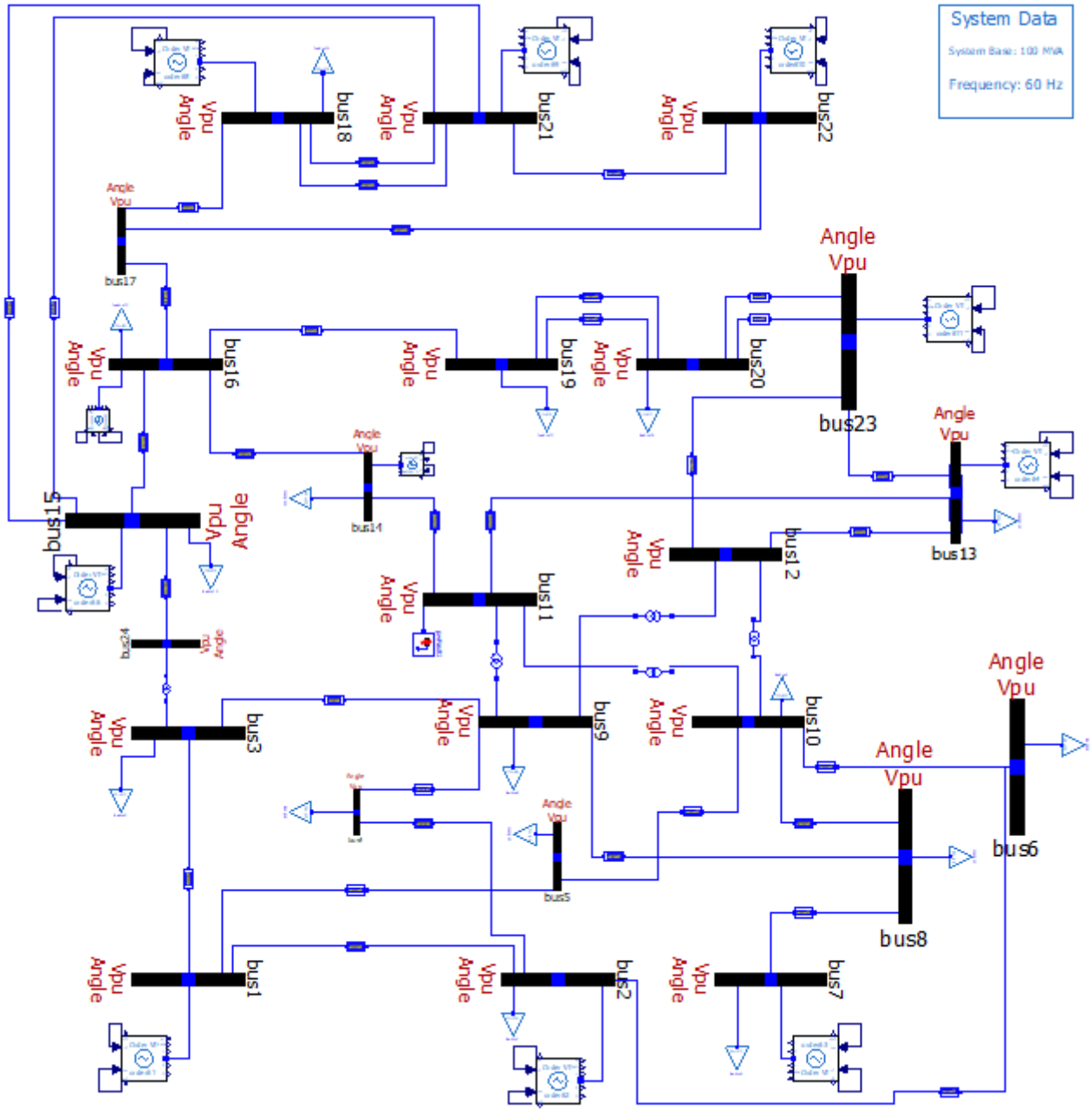

Figure 1: Implementation of IEEE 24 bus system using Modelica and OpenIPSL.

Explanation:
This model uses the following components:

Component Name	Class Path	Number
Two Winding Transformer	OpenIPSL.Electrical.Branches.PSAT.TwoWindingTransformer	5
Three phase fault	OpenIPSL.Electrical.Events.PwFault	1
Constant PQ Load	OpenIPSL.Electrical.Loads.PSAT.LOADPQ	16
Generators	OpenIPSL.Electrical.Machines.PSAT.Order6	11
Buses	OpenIPSL.Electrical.Buses.Bus	24
PwLine	OpenIPSL.Electrical.Branches.PwLine	34
Sysdata block	OpenIPSL.Electrical.SystemBase	1

Table 1: Components used in system

The IEEE reliability subcommittee developed the IEEE 24-bus test system and published in 1979 as a benchmark for testing various reliability analysis methods. The IEEE 24 bus model implemented in Modelica language using OpenIPSL package, is used to study the voltage stability at different buses. The system is on a 100 MVA base. For all analysis of this system, the lower voltage magnitude limits at all buses are 0.95 P.u. and upper limits are 1.05 P.u. The type of generator used is a synchronous motor of order6. A fault is simulated for the duration of 4 to 4.4 seconds at the 11^{th} bus. During the fault, we can observe from the bus voltage profiles, that the voltage dip is more for the 11^{th} bus as it is the fault bus and the severity of the fault decreased as we move away from the fault bus. Simulation obtained shows profiles at various buses and waveforms obtained are observed.

The simulation result of all 24 Bus voltages shown below.

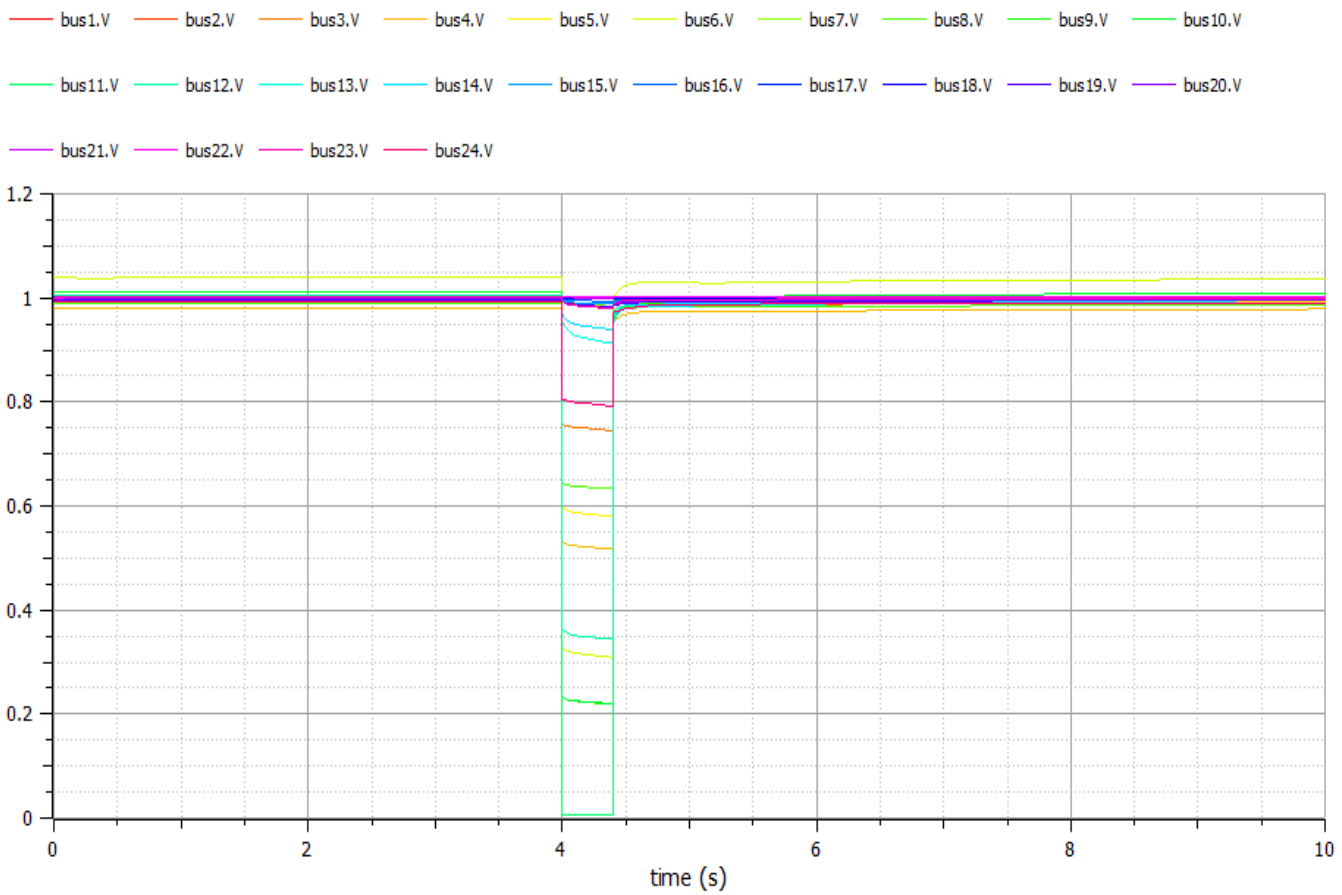

Figure 2: The voltage profiles of simulated IEEE 24 bus.

Bus no.	Bus Voltage magnitude (p.u.)
1	1.00258
2	1.00102
3	0.989827
4	0.978614
5	0.991594
6	1.03617
7	0.997514
8	0.98646
9	0.995726
10	1.00896
11	0.999833
12	1.00135
13	0.995113
14	0.995511
15	0.996981
16	0.997267
17	0.999669
18	0.999277
19	0.994917
20	0.99726
21	1.00081
22	1.00254
23	0.9995
24	0.99005

Table 2: Bus voltage magnitude (p.u.) of all buses obtained.

Conclusion:

The implemented IEEE 24 bus model in Modelica represents the system behaviour before and after the fault occurs at the 18^{th} bus. Bus voltage magnitudes (p.u.) of all 24 buses obtained are found to be between 0.95 p.u and 1.05 p.u. The relation between line impedance and fault severity observed.