

Title: Modelling of Open Circuit Fault Analysis of 11 bus system using the Open IPSL

Name of the Contributor: Aritra Banerjee

Institution/Organization: Meghnad Saha Institute of Technology, Kolkata

Email: aritrabanerjee343@gmail.com

Abstract: The IEEE 11-bus test system shall be used to study the voltage stability at different buses. The simulation represents Open Circuit Fault Analysis of 11 bus system. Open circuit faults have been simulated on standard IEEE 11 bus system. The power system model consists of 5 generators, 11 buses, 6 loads, 18 lines. The system is on a 100 MVA base. The model submitted is implemented in Modelica language using OpenIPSL package shown in Figure 1. A fault simulated at Bus 9 for the duration of 0.4 seconds (5 seconds to 5.4 seconds), the simulated voltage profiles of IEEE 11 bus system at various buses shown in Figure 2. For all analysis of this system, the lower voltage magnitude limits at all buses are 0.98 p.u and upper limits are 1.09 p.u. Simulation obtained shows voltage profiles at various buses

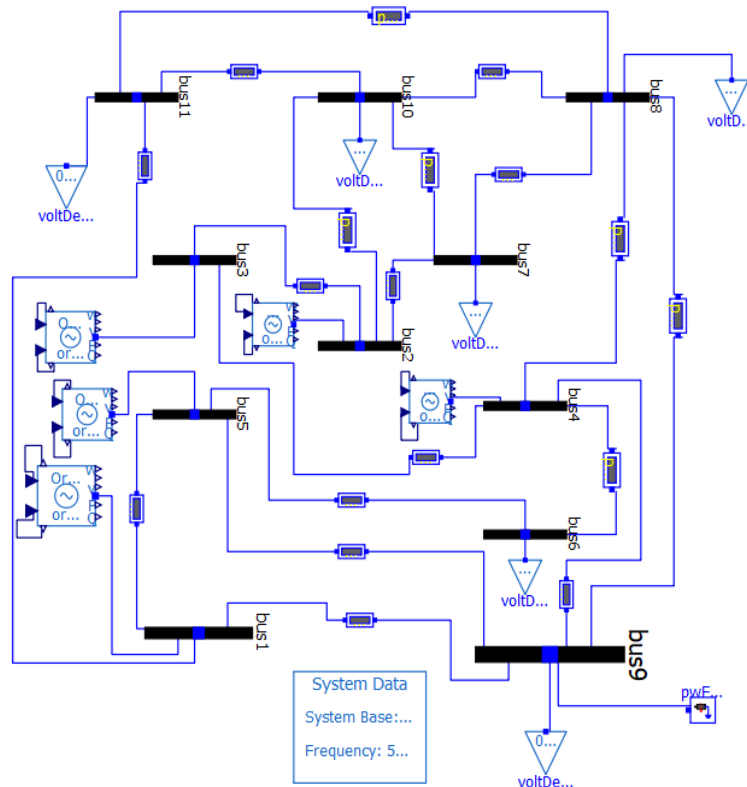


Figure 1: Implementation of IEEE 11 bus system using Modelica and OpenIPSL.

Explanation:

This model uses the following components:

Component Name	Class Path	Number
Generator (order 3)	OpenIPSL.Electrical.Machines.PSAT.Order3	5
Bus	OpenIPSL.Electrical.Buses.Bus	11
Transmission Line	OpenIPSL.Electrical.Branches.PwLine	18
Load	OpenIPSL.Electrical.Loads.PSAT.VoltDependant	6
System block	OpenIPSL.Electrical.SystemBase	1
Three phase fault	OpenIPSL.Electrical.Events.PwFault	1

The voltage profile of the system may be reduced to unacceptable limits as a result of fault. A frequency drop may lead to instability. For all analysis of this system, the lower voltage magnitude limits at all buses are 0.98 P.u. and upper limits are 1.09 P.u. The type of generator used is a synchronous motor of order3. A fault is simulated for the duration of 5 to 5.4 seconds at the 9 th bus. During the fault, we can observe from the bus voltage profiles, that the voltage dip is more for the 9th bus as it is the fault bus and the severity of the fault decreased as we move away from the fault bus. Simulation obtained shows profiles at various buses and waveforms obtained are observed.

The simulation result of all 11 Bus voltages shown below:

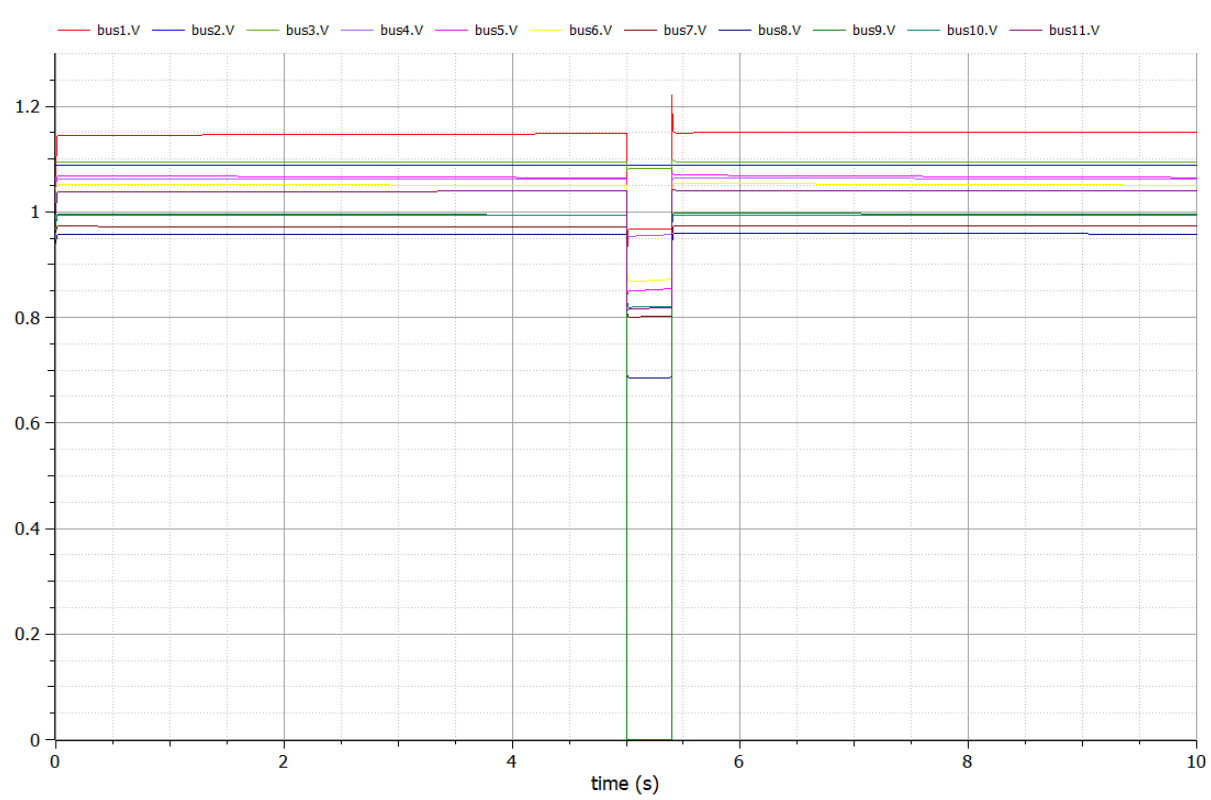


Figure 2: The voltage profiles of simulated IEEE 11 bus

BUS NUMBER	BUS VOLTAGE MAGNITUDE (p.u)
1	1.070000
2	1.089000
3	1.095000
4	1.062000
5	1.46000
6	1.050112
7	1.009529
8	0.987545
9	0.997979
10	1.030294
11	1.030067

Conclusion:

The implemented IEEE 11 bus model in Modelica represents the system behavior before and after the fault occurs at the 9 th bus. Bus voltage magnitudes (p.u.) of all 11 buses obtained are found to be between 0.98 p.u and 1.09 p.u. The relation between line impedance and fault severity observed. If there is any fault occurs in a system it can be a open circuit fault and here we observed a open circuit fault in a 11 bus system.

